AMENDMENTS TO THE SPECIFICATION

Please replace the title of the invention with the following.

PULSE-CONTROLLED TWO-PHASE ASYNCHRONOUS PIPELINE

Please replace the paragraph beginning on page 18, line 1 with the following.

Referring to **FIG. 6**, dual pulse generator **504** includes a two-input exclusive-OR (XOR) logic gate **606** receiving a data transfer control signal directly from C-element **204** at one input and a delayed data transfer control signal at the other input. The delay on the data transfer control signal is imparted by a pair of inverters **608**. Dual pulse generator ~~**604**~~ **504** produces a pulse at output node **505** on both a rising edge and a falling edge of the data transfer control signal from C-element **204**. It should be noted that a wide variety of circuit configurations are available for generating a pulse on both a rising and a falling edge input, and that the dual pulse generator incorporated within the present invention is not limited to the particular implementation depicted in **FIG. 6.**

Please replace the paragraph beginning on page 4, line 10 with the following.

There are two alternative signaling protocols available for handshaking utilizing request line **110** and acknowledge line **108**; namely a two-phase protocol and a four-phase protocol. The behavior of request line **110** and acknowledge line **108** for a four-phase micropipeline control protocol is depicted in **FIG.** ~~**2A**~~ **4A**.

Please replace the paragraph beginning on page 4, line 16 with the following.

The four-phase protocol is a return to zero protocol. **FIG.** ~~**2A**~~ **4A** illustrates the relative behavior of a request signal, *req1*, an acknowledge signal, *ack1*, and a corresponding data signal, *data1*, during a single four-phase data transfer cycle. The rising edge of *req1* signals the validity of data within sender **102** and the readiness of sender **102** to send the data. The rising edge of *ack1* indicates that the data has been received and processed by receiver **104**. It should be noted that the falling edges of *req1* and *ack1* comprise the recovery phase of the four-phase protocol during which no data transfer occurs. A widely recognized advantage of implementing a four-

phase micropipeline handshake protocol is that four-phase macromodule components are relatively simple and provide optimum latch control.